

What is claimed is:

1. A microcomputer comprising:

a central processing unit;

a high-speed serial communication interface circuit which can be utilized for a debugging interface; and

an external bus interface circuit which can be connected to an external memory,

wherein the high-speed serial communication interface circuit has a plurality of input buffers therein and data can be mutually output from one of the input buffers in parallel with an input operation to the other input buffer, and

the high-speed serial communication interface circuit receives a system program in the debugging mode and the system program thus received can be output from the external bus interface circuit together with a memory access control signal.

2. The microcomputer according to claim 1, wherein the high-speed serial communication interface circuit is a universal serial bus interface circuit.

3. The microcomputer according to claim 2, further comprising a direct memory access controller capable of carrying out a control to transfer the received system program to a memory connected to the external bus interface.

4. The microcomputer according to claim 3, wherein a transfer source of the system program through the direct memory

access controller is an input buffer of the high-speed serial communication interface.

5. The microcomputer according to claim 3, further comprising a random access memory capable of temporarily storing a system program received by an input buffer of the high-speed serial communication interface circuit,

a transfer source of the system program through the direct memory access controller being the random access memory.

6. The microcomputer according to claim 1, further comprising a debugging dedicated low-speed serial communication interface circuit, the debugging dedicated low-speed serial communication interface circuit being usable for inputting control data to control the high-speed serial communication interface circuit in the debugging mode.

7. The microcomputer according to claim 6, wherein the debugging dedicated low-speed serial communication interface circuit is usable for receiving the system program in place of the high-speed serial communication interface circuit in the debugging mode.

8. The microcomputer according to claim 6, wherein the debugging dedicated low-speed serial communication interface circuit is based on JTAG and has a data register.

9. The microcomputer according to claim 1, further comprising a trace control circuit, the trace control circuit

successively storing, as trace information, an internal state obtained when the central processing unit executes the system program.

10. The microcomputer according to claim 9, wherein the high-speed serial communication interface circuit can be utilized for an external output of the trace information.

11. A method for developing a system program which is to be executed by a target device by using a host computer, an emulator and a target device, comprising:

a first processing of storing a system program output through a high-speed serial communication by the host computer in one of two-plane buffers as a processing to be carried out by the emulator;

a second processing of transmitting a system program stored in the other buffer to the target device through a low-speed serial communication in parallel with the first processing; and

a third processing of carrying out a handshake control of the low-speed serial communication together with the target device.

12. The method for developing a system program according to claim 11, wherein the system program output from the buffer is transmitted through the low-speed serial communication to the target device via an FIFO buffer having a storage capacity which is equal to or larger than that of one of the buffers

in the second processing, and

a transmission from the FIFO buffer to the target device is carried out in response to a transmission permission sent from the target device, thereby suppressing a transfer from the buffer to the FIFO buffer in response to a full state of the FIFO buffer in the third processing.

13. A microcomputer having a user mode and a debugging mode, comprising:

a central processing unit;

a universal serial bus interface circuit;

an ROM retaining a first debugging control program;

an RAM; and

an external bus interface circuit,

wherein the universal serial bus interface circuit has a predetermined endpoint buffer circuit which can be utilized in the debugging mode, the predetermined endpoint buffer circuit has a pair of buffers which can be operated in parallel, and one of the buffers can be caused to carry out an input operation and the other buffer can be caused to carry out an output operation in parallel therewith, and

when the debugging mode is designated in a power-on reset, the central processing unit executes the first debugging control program to initialize the universal serial bus interface circuit to be operable, a second debugging control program is received by the universal serial bus interface

circuit, the second debugging control program thus received is stored in the RAM, and a transition to an execution of the second debugging control program stored in the RAM is made.

14. The microcomputer according to claim 13, further comprising a buffer RAM and a direct memory access controller,

the central processing unit causing the direct memory access controller to transfer the program received by the universal serial bus interface circuit to the buffer RAM in response to a download request command received by the universal serial bus interface circuit in accordance with the second debugging control program.

15. The microcomputer according to claim 14, wherein the central processing unit causes the direct memory access controller to carry out a control to transfer a program transmitted to the buffer RAM through an external bus interface circuit to an outside in response to a transfer request command received by the universal serial bus interface circuit in accordance with the second debugging control program.

16. The microcomputer according to claim 13, wherein the central processing unit makes a transition to the user mode in response to a mode control command in an execution state of the second debugging control program, and

the central processing unit fetches an instruction through the external bus interface circuit in the user mode.

17. A microcomputer comprising:

a central processing unit;
a universal serial bus interface circuit;
an ROM retaining a first debugging control program;
a buffer RAM; and
an external interface circuit,

wherein the universal serial bus interface circuit has a predetermined endpoint buffer circuit, the predetermined endpoint buffer circuit has a pair of buffers which can be operated in parallel, and one of the buffers can be caused to carry out an input operation and the other buffer can be caused to carry out an output operation in parallel therewith, and

in a power-on reset, the central processing unit executes the first debugging control program to initialize the universal serial bus interface circuit to be operable, a second debugging control program is received by the universal serial bus interface circuit, the second debugging control program thus received is stored in the buffer RAM, and the second debugging control program stored in the buffer RAM is output through the external interface circuit.

18. The microcomputer according to claim 17, further comprising a direct memory access controller,

the direct memory access controller transferring the second debugging control program from the buffer RAM to an outside through the external interface circuit in accordance with a transfer control condition set by the central processing

unit.